1. A method for forming for forming highly activated, ultra shallow semiconductive element of a first conductive type embedded in a semiconductive region of a second conductive type comprising:

I. providing a semiconductor substrate having an active region of said second conductive type;

(b) amorphizing an upper portion of said active region by ion implantation;

(c) implanting an impurity of said first type into said upper portion; and

(d) activating said impurity, thereby forming said semiconductive element of said second type, by pulsed laser irradiation whereby the fluence, pulse duration, and pulse frequency of said irradiation is selected to raise the local temperature of said upper portion to just below but never reaching or exceeding the melting temperature of said amorphized upper region.

2. The method of claim 1 wherein said semiconductor substrate is silicon.

3. The method of claim 2 wherein said first conductive type is p-type and said second conductive type is n-type.

4. The method of claim 1 wherein said amorphizing is performed by ion implantation of germanium or silicon ions.

5. The method of claim 4 wherein said amorphizing is performed by implanting germanium or silicon ions at a dose of between about $1x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.5 and 20 keV.

6. The method of claim 1 wherein said upper portion is between about 2 and 20 nm, thick.

7. The method of claim 3 wherein said impurity of said first type is boron implanted as boron ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.2 and 0.7 keV.

8. The method of claim 3 wherein said impurity of said first type is boron implanted as BF_2^+ ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

9. The method of claim 1 wherein said pulsed laser irradiation is performed by a 248 nm. wavelength KrF excimer laser producing radiation energy at a fluence of between about 0.1 and 0.8 Joules/cm^2 in pulses of between about 10 and 40 ns. duration, applied at a repetition rate of about 1Hz.

10. The method of claim 9 wherein at least 10 pulses are applied.

11. The method of claim 2 wherein said first conductive type is n-type and said second conductive type is p-type.

12. The method of claim 11 wherein said impurity of said first type is phosphorous implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 2 and 10 keV.

13. The method of claim 11 wherein said impurity of said first type is arsenic implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

14. A method for forming a MOSFET device having ultra shallow lightly doped source/drain extensions, comprising:

1. providing a semiconductor substrate having an active region of a first conductive type enclosed by field isolation;

(b) forming a gate oxide on said active region;

(c) forming a gate electrode on said gate oxide, thereby defining source/drain regions separated by a gate stack;

(d) amorphizing an upper portion of said source/drain regions by ion implantation;

(e) implanting a first dose of an impurity of a second type into said upper portion;

(f) forming source/drain extensions by activating said impurity of said second type by pulsed laser irradiation whereby the fluence, pulse duration, and pulse frequency of said irradiation is selected to raise the local temperature of said upper portion to just below but never reaching or exceeding the melting temperature of said amorphized upper region;

(g) forming sidewalls alongside said gate stack; and

(h) implanting a second dose of an impurity of said second type thereby forming source/drain contact elements.

15. The method of claim 14 wherein said semiconductor substrate is silicon.

16. The method of claim 14 wherein said amorphizing is performed by ion implantation of germanium or silicon ions.

17. The method of claim 16 wherein said amorphizing is performed by implanting germanium or silicon ions at a dose of between about $1x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.5 and 20 keV.

18. The method of claim 14 wherein said upper portion is between about 2 and 20 nm, thick.

19. The method of claim 15 wherein said first conductive type is n-type and said second conductive type is p-type.

20. The method of claim 15 wherein said impurity of said second type is boron implanted as boron ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.2 and 0.7 keV.

21. The method of claim 15 wherein said impurity of said second type is boron implanted as BF_2^+ ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

22. The method of claim 14 wherein said pulsed laser irradiation is performed by a 248 nm. wavelength KrF excimer laser producing radiation energy at a fluence of between about 0.1 and 0.8 Joules/cm^2 in pulses of between about 10 and 40 ns. duration, applied at a repetition rate of about 1Hz.

23. The method of claim 22 wherein at least 10 pulses are applied.

24. The method of claim 15 wherein said first conductive type is p-type and said second conductive type is n-type.

25. The method of claim 24 wherein said impurity of said second type is phosphorous implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 2 and 10 keV.

26. The method of claim 24 wherein said impurity of said second type is arsenic implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

27. The method of claim 14 wherein said gate electrode is formed of polysilicon.

28. The method of claim 14 wherein said source/drain elements extend below said amorphized region

29. A method for forming a CMOS device having ultra shallow lightly doped source/drain extensions, comprising:

9. providing a semiconductor substrate having an n-type active region and a p-type active region, each of said active regions enclosed by field isolation;

(j) forming a gate oxide on each of said active regions;

(k) forming a first gate electrode on said gate oxide on said n-type active region and a second gate electrode on said gate oxide on said p-type active region, thereby defining first source/drain regions separated by a first gate stack on said n-type active

region and second source drain regions separated by a second gate stack on said p-type active region;

(l) amorphizing an upper portion of each of said source/drain regions by ion implantation;

(m) patterning a first layer of photoresist on said wafer to form a first blockout mask protecting said second source/drain regions;

(n) implanting a first dose of a p-type impurity into said upper portion of said first source/drain regions;

(o) striping said first blockout mask;

(p) patterning a second layer of photoresist on said wafer to form a second blockout mask protecting said first source/drain regions;

(q) implanting a first dose of an n-type impurity into said upper portion of said second source/drain regions;

(r) striping said second blockout mask;

(s) forming sidewalls alongside each of said first and second gate stacks;

(t) patterning a third layer of photoresist on said wafer to form a third blockout mask protecting said second source/drain regions;

(u) implanting a second dose of a p-type impurity into said upper portion of said first source/drain regions;

(v) striping said third blockout mask;

(w) patterning a fourth layer of photoresist on said wafer to form a fourth blockout mask protecting said first source/drain regions;

(x) implanting a second dose of an n-type impurity into said upper portion of said second source/drain regions;

(y) striping said fourth blockout mask;

(z) forming source/drain contact elements with extensions by activating said first and second doses of said p-type impurity and said first and second doses of said n-type impurity by pulsed laser irradiation whereby the fluence, pulse duration, and pulse frequency of said irradiation is selected to raise the local temperature of said upper portion to just below but never reaching or exceeding the melting temperature of said amorphized upper region; and

(aa) forming silicide contact on each of said source/drain contact elements and on each of said gate stacks.

30. The method of claim 29 wherein said semiconductor substrate is silicon.

31. The method of claim 29 wherein said amorphizing is performed by ion implantation of germanium or silicon ions.

32. The method of claim 29 wherein said amorphizing is performed by implanting germanium or silicon ions at a dose of between about $1x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.5 and 20 keV.

33. The method of claim 29 wherein said upper portion is between about 2 and 20 nm, thick.

34. The method of claim 29 wherein said first dose of said p-type impurity is boron implanted as boron ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 0.2 and 0.7 keV.

35. The method of claim 29 wherein said first dose of said p-type impurity is boron implanted as BF_2^+ ions at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

36. The method of claim 29 wherein said first dose of said n-type impurity is phosphorous implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 2 and 10 keV.

37. The method of claim 29 wherein said first dose of said n-type impurity is arsenic implanted at a dose of between about $5x10^{14}$ and $1x10^{16}$ ions/cm^2 at an energy of between about 5 and 30 keV.

38. The method of claim 29 wherein said source/drain contact elements extend below said amorphized region.